



UNI-SEMICONDUCTOR CO., LTD

宇力半导体有限公司



## AP120N04K Data Sheet

V 1.1

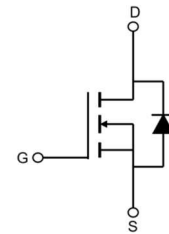
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## Feature

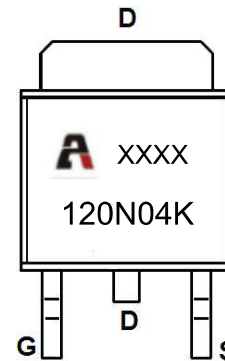
- 40V,120A  
 $R_{DS(ON)} < 3.5m\Omega @ V_{GS}=10V$   
 $R_{DS(ON)} < 5.5m\Omega @ V_{GS}=4.5V$
- Advanced Trench Technology
- Lead free product is acquired
- Excellent  $R_{DS(ON)}$  and Low Gate Charge

## Application

- PWM applications
- Load Switch
- Power management



Schematic Diagram



Marking and pin assignment

## Package Marking and Ordering Information

| Device Marking | Device    | Device Package | Reel Size | Tape width | Quantity (PCS) |
|----------------|-----------|----------------|-----------|------------|----------------|
| 120N04K        | AP120N04K | TO-252         | 13 inch   | -          | 2500           |

## ABSOLUTE MAXIMUM RATINGS ( $T_a=25^\circ\text{C}$ unless otherwise noted)

| Parameter  | Symbol          | Value     | Unit                      |
|--|-----------------|-----------|---------------------------|
| Drain-Source Voltage                                 | $V_{DS}$        | 40        | V                         |
| Gate-Source Voltage                                  | $V_{GS}$        | $\pm 20$  | V                         |
| Continuous Drain Current ( $T_a=25^\circ\text{C}$ )  | $I_D$           | 120       | A                         |
| Continuous Drain Current ( $T_a=100^\circ\text{C}$ ) | $I_D$           | 78        | A                         |
| Pulsed Drain Current <sup>(1)</sup>                  | $I_{DM}$        | 480       | A                         |
| Singel Pulsed Avalanche Energy <sup>(2)</sup>        | $E_{AS}$        | 150       | mJ                        |
| Power Dissipation                                    | $P_D$           | 108       | W                         |
| Thermal Resistance from Junction to Case             | $R_{\theta JC}$ | 1.4       | $^\circ\text{C}/\text{W}$ |
| Junction Temperature                                 | $T_J$           | 150       | $^\circ\text{C}$          |
| Storage Temperature                                  | $T_{STG}$       | -55~ +150 | $^\circ\text{C}$          |

Test Circuit

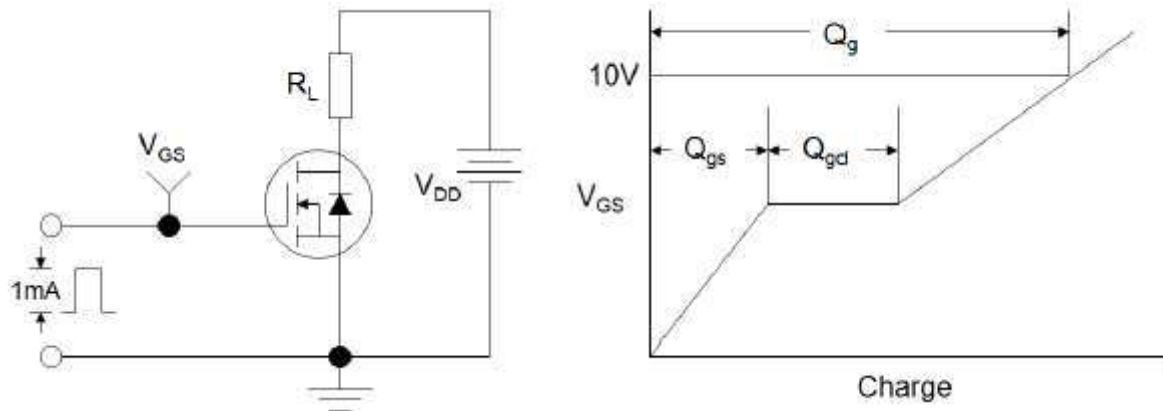


Figure1:Gate Charge Test Circuit & Waveform

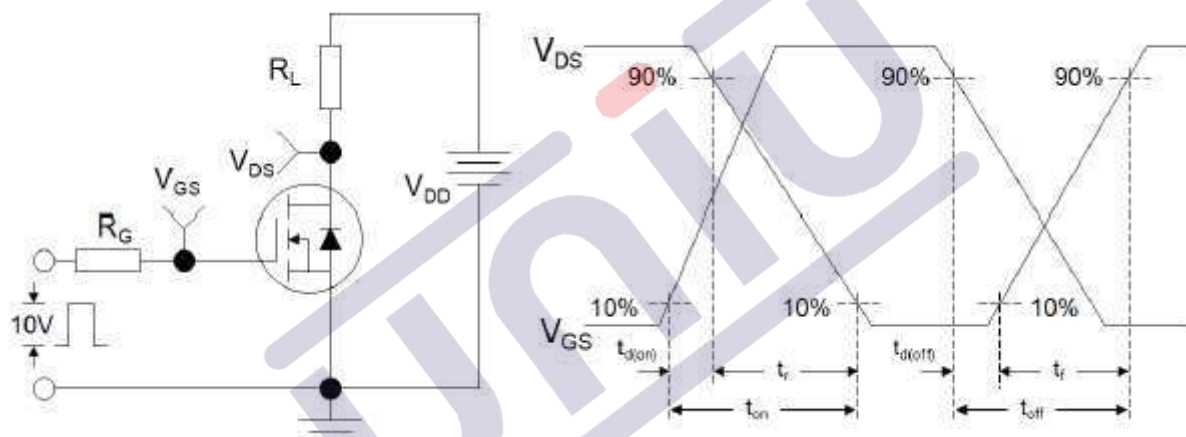


Figure 2: Resistive Switching Test Circuit & Waveforms

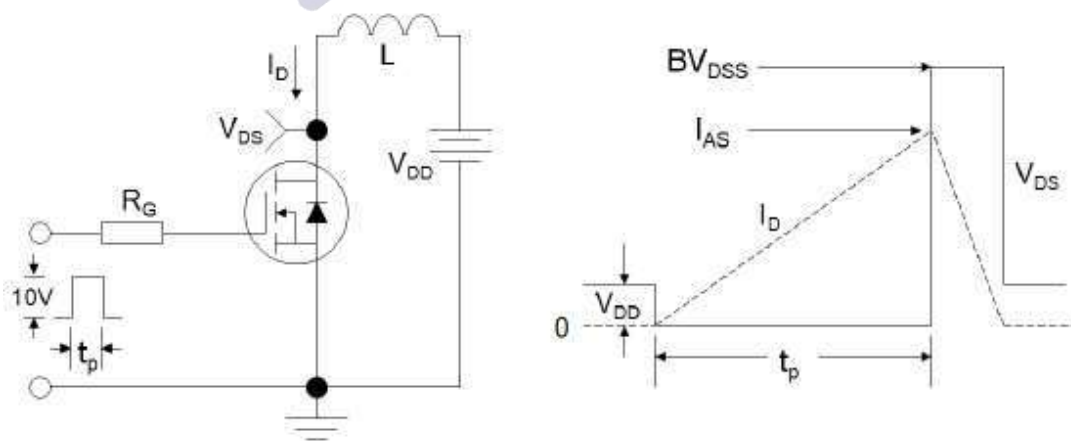


Figure 3:Unclamped Inductive Switching Test Circuit & Waveforms

## 1.版本记录

| DATE       | REV. | DESCRIPTION       |
|------------|------|-------------------|
| 2018/07/14 | 1.0  | First Release     |
| 2019/07/13 | 1.1  | Layout adjustment |
|            |      |                   |

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